The Application of a Frequency Multiplier Design Method to the Design of Microwave Parametric Dividers

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Abstract—**A practical and efficient design method for microwave frequency dividers is described. The approach is based on the analogy between frequency multipliers and dividers at the same conditions of power levels and operating frequency. Hence, the well-known practical design procedure for frequency doublers, using published dynamic varactor parameters, may be used for designing frequency dividers.**

I. Introduction

PARAMETRIC frequency dividers using varactors are useful in many system applications owing to their superior performance and much simpler circuit configuration compared to other regenerative circuits. The basic theory of device operation is presented in [1] and [2]. Divider designs based on empirical techniques are described in [3] and [4] and are analyzed in [5]. A design approach that outlined the CAD of nonlinear circuits [6] is still not user oriented for practical applications.

Although the treatment in [2] of a divider circuit using a varactor is similar at steady state to that of a frequency multiplier, its application to divider design has yet not been published.

This work points out the analogy and equivalence between frequency multipliers and dividers from a design point of view. The steady-state operation of varactor doubler and halver circuits is described, leading to the same large-signal equations and the same dynamic impedances of the varactor in both circuits. It is shown that the circuit conditions necessary for frequency division fit the circuit configuration of varactor multipliers when run backwards. A practical and efficient approach for the design of varactor halvers based on the analogy between varactor multipliers and dividers is presented. The method is demonstrated by a practical design of a varactor halver, applying the well-known design concepts for varactor doublers.

II. Analogy Between Divider and Multiplier Circuits

When generating subharmonics of the driving frequency, varactors behave much like oscillators. As the output current builds up, nonlinear effects reduce the rate of amplitude rise, and finally a steady state with a constant output power is reached. The analysis here treats the large-signal steady state of a doubler and a divide-by-two (halver) circuit, and the necessary conditions for frequency division to occur in a varactor are discussed. Finally, it will be shown that this treatment can support the growth of oscillations at the subharmonic frequency.

For the divider circuit in Fig. 1(a), we assume that the currents are allowed to flow only at the driving frequency $f_p = 2f_o$ and the output frequency f_o. A similar circuit is shown for a doubler in Fig. 1(b), except that the driving source and load are interchanged.

The varactor is described by the circuit model shown in Fig. 2, where C is a nonlinear voltage-dependent junction capacitance given below in (1), R_s is a series resistance (assumed constant), and L_s and C_p are the package parasitics. The well-known expression for the $C-v$ characteristics of the varactor is

$$C = C_{\min}\left(\frac{v+\phi}{V_B+\phi}\right)^{-\gamma} \tag{1}$$

where

- v voltage across the junction,
- V_B breakdown voltage,
- ϕ contact potential,
- γ constant.

The steady-state equations for the doubler and halver circuits are presented in [2]. These are large-signal equations for the voltages V_1 at f_o and V_2 at $2f_o$ as functions of the currents I_1 at f_o and I_2 at $2f_o$. These equations are derived from the more general form obtained from Fig. 2:

$$V(t) = R_s I(t) + \int S(t) I(t)\, dt \tag{2}$$

where

- V total voltage on the diode,
- I diode current,
- S $1/C$ incremental elastance.

These can be expressed in the form

$$V(t) = \sum_{k=-\infty}^{+\infty} V_k e^{jk\omega_o t} \tag{3}$$

$$I(t) = \sum_{k=-\infty}^{+\infty} I_k e^{jk\omega_o t} \tag{4}$$

$$S(t) = \sum_{k=-\infty}^{+\infty} S_k e^{jk\omega_o t} \tag{5}$$

where $\omega_o = 2\pi f_o$.

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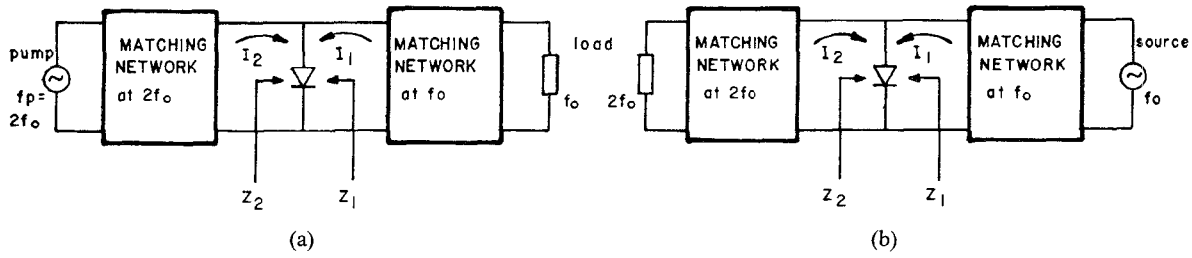

Fig. 1. (a) General description of a parametric frequency divider. (b) General description of a frequency multiplier.

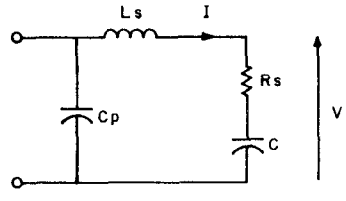

Fig. 2. Circuit model of a packaged varactor diode.

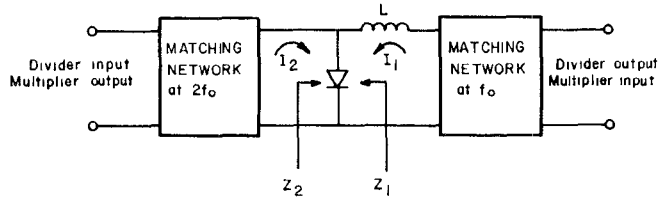

Fig. 3. General circuit of a varactor multiplier or divider.

The analysis in [2] is restricted to the abrupt-junction varactor ($\gamma = \frac{1}{2}$), for which S is proportional to the charge q (time integral of the current). From (2), each Fourier coefficient V_k ($k = 1,2$) can be expressed in terms of I_1, I_2 and S_1, S_2 (assuming the circuit allows varactor currents at $f_o, 2f_o$ only). Thus, the same closed-form steady-state equations for the doubler and halver are obtained:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} R_s + \dfrac{S_o}{j\omega_o} & \dfrac{S_1^*}{j2\omega_o} \\ \dfrac{S_1}{j2\omega_o} & R_s + \dfrac{S_o}{j2\omega_o} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}. \tag{6}$$

Let Z_1 and Z_2 be the dynamic impedances of the varactor at f_o and $2f_o$ as defined in (a) and (b) of Fig. 1. Then

$$V_1 = Z_1 I_1 \tag{7}$$

$$V_2 = Z_2 I_2. \tag{8}$$

This treatment leads to the same closed-form solution for Z_1 and Z_2 in a doubler or a halver (the same is true for the bias voltage, efficiency, etc.). In principle, the same concept holds for other types of varactors of different characteristics.

Many works have been published concerning the characterization of varactors of different types for frequency multiplier design [7], [8]. The general expressions for the varactor impedances are of the form

$$Z_1 = \frac{\bar{R}_1}{\omega_o C_{\min}} - j\frac{\bar{X}_1}{\omega_o C_{\min}} \tag{9}$$

$$Z_2 = \frac{\bar{R}_2}{\omega_o C_{\min}} - j\frac{\bar{X}_2}{\omega_o C_{\min}} \tag{10}$$

where $\bar{R}_1$ and $\bar{R}_2$ are the normalized real parts of the varactor impedances at f_o and $2f_o$ and $\bar{X}_1$ and $\bar{X}_2$ are the normalized imaginary parts. These normalized parameters, which depend on the γ of the varactor's $C-v$ characteristics and drive level, are given in useful design tables in [7] and [8]. These parameters were calculated at the maximum efficiency bias voltage for the $C-v$ characteristics and drive levels of various varactors. Therefore, from the steady-state-operation point of view, those tables may be useful for designing frequency dividers, applying the same design techniques and circuit configuration concepts as proposed for doublers.

Like other nonlinear reactances, varactors can, when pumped, generate power not only at harmonics of the pumping frequency but also at subharmonics. Any nonlinear device can generate harmonics of the driving frequency, but some of them cannot generate subharmonics. In particular, the previous works mentioned in [2] show that nonlinear resistance doublers will not function as halvers.

Now we have to point out the necessary conditions for frequency division to occur in a varactor, and its dynamic range behavior as a halver.

The power output at frequency ω_o is

$$P_{\text{out}} = -2\,\text{Re}\,V_1 I_1^*. \tag{11}$$

Then, from (6), we obtain for the abrupt-junction varactor (assuming $S_1^*/S_2 = -2I_1^*/I_2$)

$$P_{\text{out}} = 2|I_1|^2\left(\frac{|S_2|}{\omega_o}\cos\theta - R_s\right) \tag{12}$$

where

$$\theta = \angle S_2 - \frac{\pi}{2} - 2\angle I_1.$$

Power can be drawn from the varactor at frequency ω_o only if the expression in the parentheses of (12) is positive. Therefore, the circuit is phase-sensitive. Following [2], we can show from (6) and (7) that, if the imaginary part of the load impedance Z_1 is tuned, then $\cos\theta = 1$. Hence, power is delivered at frequency ω_o if

$$\omega_o < \frac{|S_2|}{R_s} \tag{13}$$

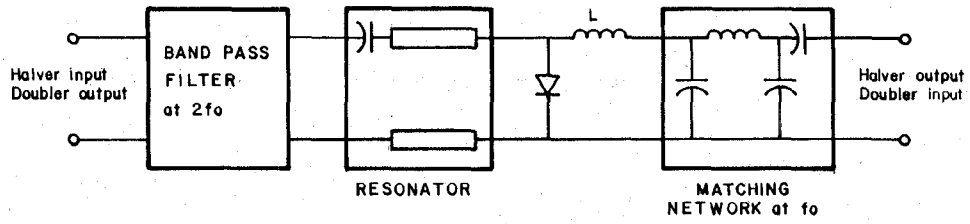

Fig. 4. Circuit topology of a multiplier or divider.

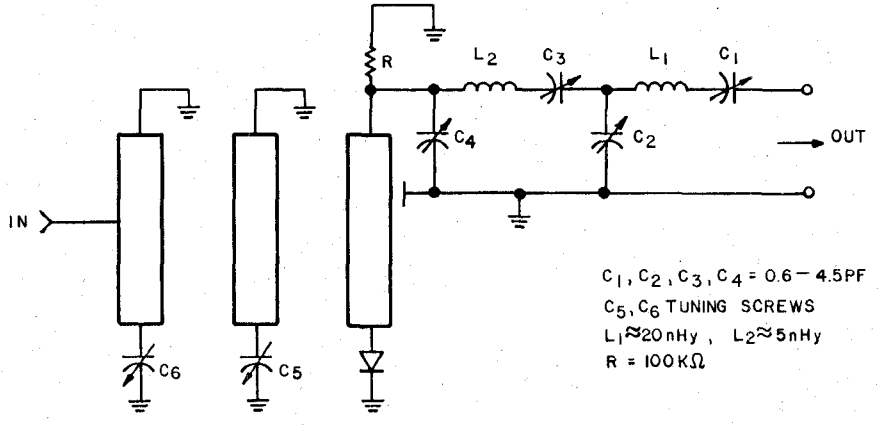

Fig. 5. Electronic circuit drawing of a divider.

otherwise, the device cannot operate as a halver. Whenever condition (13) is satisfied, oscillations, which are at one of two possible phases that differ by 180°, can occur.

These results explain the dynamic range behavior of the halver. A minimum level of input power is required to overcome the series resistance loss R_s if there is to be any subharmonic oscillation. Increasing the input power increases S_2 to satisfy (13). On the other hand, there is a maximum level of input power if the breakdown limit is not to be exceeded, a limitation that also exists for doublers. The two possible phases of oscillations in a halver result in a hysteresis curve, as reported in [4].

We must now find the circuit conditions for growing oscillations, assuming that condition (13) is fulfilled, and show that doubler circuit configuration concepts can support the buildup of parametric oscillations at the subharmonic frequency.

The small-signal current is assumed to be of the form

$$i(t) = I_1 e^{st} + I_1^* e^{s^* t} \tag{14}$$

where s is a complex frequency

$$s = \sigma + j\omega_o. \tag{15}$$

If σ, the real part of s, is positive, the oscillations grow. Since σ determines the rate of growth, we have to find the circuit conditions to maximize σ.

As discussed in [2], the only condition to support growing oscillations which depends on the circuit itself is the requirement of an inductance L that resonates the varactor at frequency s.

This inductance appears in series with the varactor at the divider's output network, as shown in Fig. 3. The

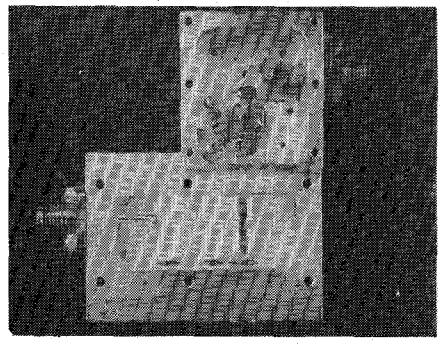

Fig. 6. Actual view of a divider circuit.

optimal expression obtained for L, which maximizes the rate of growth σ, is [2]

$$L = \frac{S_0 - |S_2|\dfrac{\sigma}{\omega_o}}{\omega_o^2 + \sigma^2} \tag{16}$$

where S_0, S_2 are the $S_k (k = 0,2)$ in (5).

If S_2 is small, the inductance L tunes out the average capacitance of the varactor (Fig. 2) at frequency $s = \sqrt{\omega_o^2 + \sigma^2}$. This value of L, which optimizes s, causes the current $i(t)$ in (14) to grow fast. At the steady state, this optimization (which results in tuning of $\mathrm{Im}(Z_1)$) determines the phase of I_1 in (12) such that $\cos\theta = 1$, which maximizes P_{out} at ω_o. However, such an inductor, which supports growing oscillations at the subharmonic frequency, also exists in varactor multipliers circuits [9], as described in Fig. 3. Hence, doubler design techniques and circuit configuration seem to be a practical, efficient solution for application in divider design.

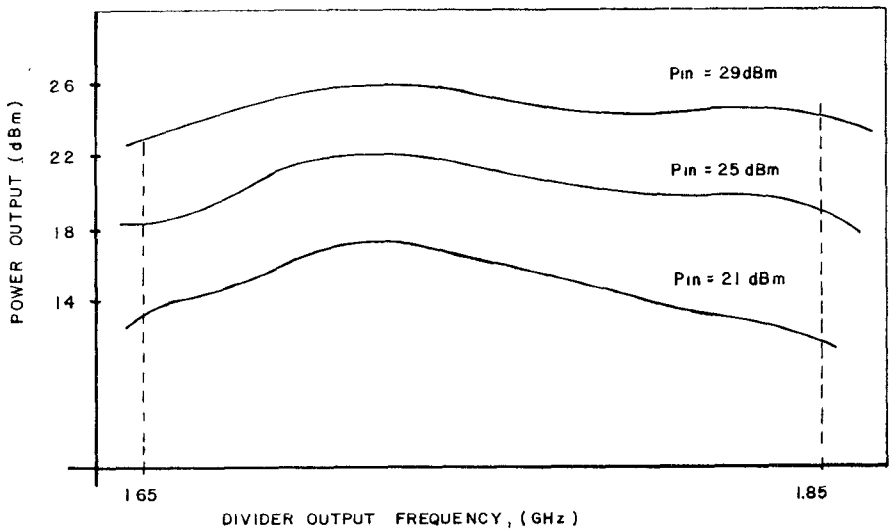

Fig. 7. Frequency response at $f_o = \frac{1}{2} f_{in}$ and the dynamic range behavior of the divider.

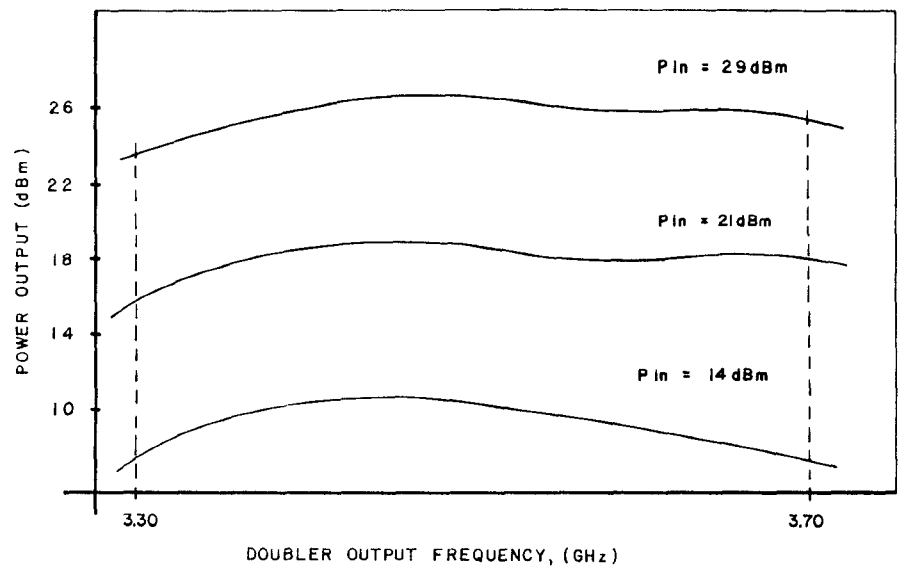

Fig. 8. Frequency response and dynamic range of the reversed halver circuit tested as a doubler (without retuning).

III. A Design Example

To demonstrate the proposed method, a design of a practical halver is described. The circuit was designed by applying doubler design methods at the required working frequency. The design goals were an input center frequency $f_{in} = 2f_o = 3.5$ GHz and a bandwidth of at least 10 percent.

The circuit consists of an input network which should act as a matching network of the bandpass type and also provide isolation between the pump signal and the signals generated by the diode. This network is a comb-line type which covers the required bandwidth centered at 3.5 GHz.

The output network is a lumped matching network of the bandpass type that passes only the output frequency f_o. The input/output networks match the low impedances of the varactor to 50 Ω at the input and output frequencies. Those dynamic impedances are calculated from the table given for doublers in [7] as follows. The expressions for the varactor impedances are given in (9) and (10); these contain normalized parameters depending on the γ of the varactor and the drive level. The tables in [7] contain optimal normalized parameters that were calculated for doublers (and also for higher multiplication factors) at the maximum efficiency bias voltage, for various γ and drive levels. The average varactor's γ in this example was found using (1) and the measured $C-v$ characteristics.

The design of the matching input/output networks is accomplished by a simple, straightforward CAD using the well-known circuit topology proposed for multipliers [9] described in Fig. 4. This circuit configuration was realized with commercial multiplier devices, such as SRD or so-called bimode varactors [8].

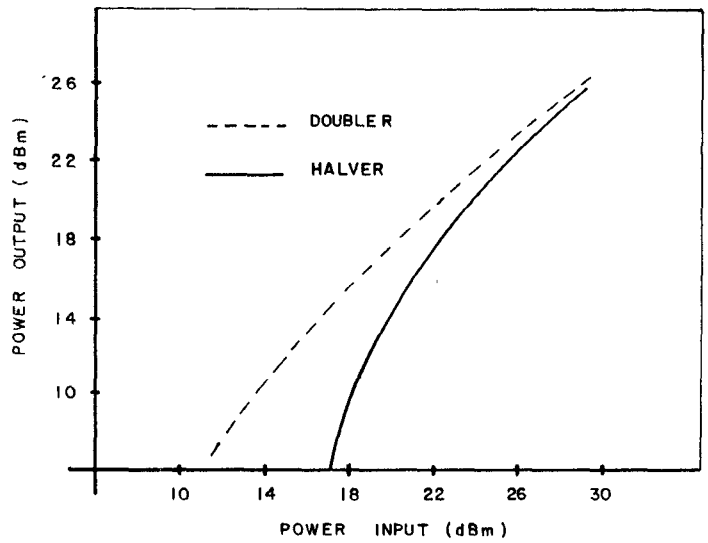

Fig. 9. Output power versus input power for the circuit tested as both a halver and a doubler.

The matching network at $2f_o$, as shown previously in Fig. 3, is separated here into its two functions: a resonator and a bandpass filter. Practically, since the varactor is a two-port device, it is likely to realize the resonator at the halver's input as part of the inductance L at the output. This concept results in a more compact design, as realized in this design example.

A schematic diagram of the frequency halver is shown in Fig. 5. The diode used in this example is a MA-44705 multiplier silicon varactor with a self-bias arrangement. The circuit was built in a coaxial structure in which tuning capacitors were used to tune the circuit for optimum performance. The actual structure of the divider is shown in Fig. 6.

IV. Measured Results

A minimum level of input power P_{in} is required in order for frequency division to occur. For this divider, the threshold input level is about 17–18 dBm, at which frequency division commences abruptly. As P_{in} increases beyond this level, the bandwidth increases.

The output frequency response and the dynamic range behavior of the divider tested at $P_{in} = 25$ dBm ($\pm \frac{1}{2}$dB) are shown in Fig. 7. As shown, a reasonable conversion loss of 3–6 dB is obtained, with a dynamic range of 8 dB and a bandwidth of about 10 percent. The only measured spurious signal at the output is at f_{in}, which was about 40 dB below the $\frac{1}{2}f_{in}$ output signal.

The halver circuit was tested as a doubler by reversing its input/output ports. It is interesting to point out that the circuit functioned as a doubler of similar conversion loss and had the same bandwidth as the halver, without any retuning. Its performance as a doubler is shown in Fig. 8.

The main difference in performance between the two functions of the circuit is the dynamic range behavior. As a doubler, the circuit has a much wider dynamic range and there is no threshold level of input power, as observed for the halver. The output power (max) versus input power for the design example tuned as a halver and tested as both a halver and a doubler is shown in Fig. 9. On the other hand, it should be pointed out that varactor doublers will function as halvers only if the required circuit and operating conditions are fulfilled.

V. Conclusions

A practical and efficient approach for the design of a microwave frequency divider has been demonstrated. Using this method, a halver was designed and built. A 3-dB bandwidth of about 10 percent with a maximum conversion loss of 6 dB, a dynamic range of 8 dB, and spurious signals below -40 dBc have been obtained. The design method is based on the analogy between frequency multipliers and dividers, applying the existing design techniques and circuit configuration for doublers, for the design of halvers. When reversed, the circuit functions as a doubler.

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